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10/733,226	12/10/2003	William M. Hiatt	10829874US	8010

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EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
11/27/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/733,226	HIATT ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-37,39-47 and 49-52* is/are pending in the application.

4a) Of the above claim(s) *37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-36,39-47,49-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 28 and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 6,459,150 to Wu et al. (Wu).

Re claim 28: Wu discloses a packaged microelectronic device comprising:

a die (Fig 2A-2G, element 50) having a first side (56) and a second side opposite to the first side, the die further having

an integrated circuit (col 1 lines 54-55) positioned between the first and second sides;

a bond-pad (58) positioned on the first side of the die and electrically coupled to the integrated circuit;

a passage (70) extending completely through the die and aligned with and extending through the bond-pad (see Fig 2C);

a first conductive material (90) deposited in a first portion of the passage adjacent to the first side of the die to form a conductive plug electrically connected to the bond-pad (see Fig 2F); and

a second conductive material (92) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the die (see Fig 2G).

Re claim 44: Wu discloses a microelectronic device set comprising:

a first microelectronic device (Fig 3A-3F) having:

a first die (80) with a first integrated circuit (col 8 line 48) and a first bond-pad (82) electrically coupled to the first integrated circuit, the first die further including a passage (76) aligned with and extending through the first bond-pad (see Fig 3B); and

a conductive interconnect (90/92) deposited in the passage, the conductive interconnect including a first conductive material (90) deposited in a first portion of the passage to form a conductive plug in contact with the bond-pad (see Fig 3E), and a second conductive material (92) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage (see Fig 3F); and

at least a second microelectronic device having a second die (50) with a second integrated circuit (col 1 lines 54-55) and a second bond-pad (58) electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the first bond-pad of the first microelectronic device (see Fig 3F).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29-30, 33, 36, 39-41, 43, 45 and 49-52 rejected under 35 U.S.C. 103(a)

as being unpatentable over U.S. Pat. No. 6,459,150 to Wu et al. (Wu) in view of U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka).

Re claim 33: Wu discloses a microfeature workpiece (Fig 2A-2G) having a first side (56) and a second side opposite to the first side, the microfeature workpiece comprising:

at least one die (62);

a bond-pad (58)formed on the first side of the microfeature workpiece;

a passage (70) extending completely through the bond-pad and the die from the first side of the microfeature workpiece to the second side of the microfeature workpiece (see Fig 2C);

a first conductive material (90) deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece to form a conductive plug in contact with the bond-pad (see Fig 2F); and

a second conductive material (92) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the microfeature workpiece (see Fig 2G).

Wu fails to teach wherein the first conductive material is different than the second conductive material. Hayasaka teaches a passage (Fig 17A,17B, for example) through die (10) with a first conductive material (15: W, Mo, Ni, Ti or their silicides; col 12 lines 55-60) deposited in a first portion of the passage to form a conductive plug and a

second conductive material (8: solder; col 8 lines 1-5) in contact with the conductive plug wherein the first conductive material (15: W, Mo, Ni, Ti or their silicides; col 12 lines 55-60) is different than the second conductive material (8: solder; col 8 lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to have the first conductive material different than the second conductive material as taught by Hayasaka

Re claim 39: Wu discloses a microelectronic device set comprising:

a first microelectronic device (Fig 3A-3F, 80) having:

a first die (80) with a first integrated circuit (col 8 line 48) and a first bond-pad (82) electrically coupled to the first integrated circuit, the first die further including a passage (76) extending completely through the first die and the first bond-pad (see Fig 3B); and

a conductive interconnect (90/92) deposited in the passage, the conductive interconnect including a first conductive material (90) deposited in a first portion of the passage to form a conductive plug (see Fig 3E) having a boundary in the passage, and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage (see Fig 3F); and

at least a second microelectronic device having a second die (50) with a second integrated circuit (col 1 lines 54-55) and a second bond-pad (58) electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the conductive interconnect of the first microelectronic device (see Fig 3F).

Wu fails to explicitly disclose the second conductive material in contact with the boundary of the conductive plug. Hayasaka teaches a passage (Fig 17A,17B, for example) through die (10) with a first conductive material (15: W, Mo, Ni, Ti or their silicides; col 12 lines 55-60) deposited in a first portion of the passage to form a conductive plug having a boundary insulate the passage and a second conductive material (8: solder; col 8 lines 1-5) in contact with the boundary of the conductive plug. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to have the first conductive material different than the second conductive material as taught by Hayasaka in order to prevent device degradation of due to diffusion of the conductive material (Hayaska col 14 lines 40-47)..

Re claim 40: Wu discloses the microelectronic device set of claim 39 wherein the first microelectronic device is attached to the second microelectronic device in a stacked-die arrangement (see Fig 3F).

Re claim 41: Wu discloses the microelectronic device set of claim 39, further comprising a solder ball (100) disposed between the conductive interconnect of the first microelectronic device and the second bond-pad of the second microelectronic device to electrically couple the first bond-pad to the second bond-pad (see Fig 3F).

Re claim 43: Wu discloses the microelectronic device set of claim 39 wherein the first microelectronic device (80) further includes a redistribution layer (optional layer 64, shown in Fig 2D) formed on the first die, the redistribution layer including a conductive line having a first end portion attached to the first bond-pad and a second end portion positioned outward of the first end portion, wherein the second end portion is configured

to receive electrical signals and transmit the signals to at least the first integrated circuit of the first die and the second integrated circuit of the second die (col 8 lines 31-39).

Re claims 29, 36, 45: Wu discloses packaged microelectronic device of claims 28, 33, and 44 as above. Wu fails to disclose an insulative layer deposited in the passage between the die and the first and second conductive materials. Hayasaka teaches (Fig 17A and 17B) an insulative layer (14) deposited in the passage between the die (10) and the first and second conductive materials (15 & 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to include the insulative layer as taught by Hayasaka in order to insulate the die from the via to prevent short circuiting.

Re claim 30: Wu discloses packaged microelectronic device of claim 39 as above. Wu fails to disclose an insulative layer deposited in the passage between the first die and the first and second conductive materials. Hayasaka teaches (Fig 17A and 17B) an insulative layer (14) deposited in the passage between the first die (10) and the first and second conductive materials (15 & 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to include the insulative layer as taught by Hayasaka in order to insulate the die from the via to prevent short circuiting.

Re claims 49-52: The packaged microelectronic device of claims 28, 33, 39 and 44 wherein the second conductive material contacts the conductive plug. Wu fails to disclose an insulative layer deposited in the passage, wherein the second conductive material contacts the insulative layer. Hayaska teaches (Fig 17A-17B) an insulative

layer (14) deposited in the passage, wherein the second conductive material (8) contacts the conductive plug (15) and the insulative layer (14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to include the insulative layer as taught by Hayasaka in order to insulate the die from the via to prevent short circuiting.

Claims 31, 34 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,459,150 to Wu et al. (Wu) in view of U.S. Pub. No. 2004/0087441 to Hirakata et al. (Hirakata) or U.S. Pat. No. 6,459,150 to Wu et al. (Wu) in view of U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pub. No. 2004/0087441 to Hirakata et al. (Hirakata)

Regarding claims 31, 34 and 46, Wu discloses the device of claims 28, 33 and 44 as above including the first conductive material in contact with an exposed surface of the bond-pad. Wu fails to disclose wherein the first conductive material includes an electronic ink. Hirakata teaches a first conductive material (conductive paste; paragraph 102) includes an electronic ink (ink jetting; paragraph 102) in contact with an exposed surface of the bond-pad. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first conductive material including electronic ink as taught by Hirkata because with electronic printing processes the plug only needs to be formed in the desired area therefore wasted material is reduced.

Claims 32, 35 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,459,150 to Wu et al. (Wu) in view of U.S. Pub. No. 2004/0087441 to Bock et al. (Bock) or or U.S. Pat. No. 6,459,150 to Wu et al. (Wu) in view of U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pub. No. 2004/0087441 to Bock et al. (Bock).

Regarding claims 32, 35 and 47, Wu discloses the device of claims 28, 3 and 44 as above including the first conductive material in contact with an exposed surface of the bond-pad. Wu fails to disclose wherein the first conductive material includes a nano-particle deposition. Bock teaches using a nano-particle process to deposit a conductive material (abstract lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to have the first conductive material includes a nano-particle deposition as in Bock in order to deposit fine features.

Claims 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,459,150 to Wu et al. (Wu) in view of U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 6,982,487 to Kim et al. (Kim)

Re claim 42: Wu discloses the microelectronic device set of claim 39 wherein the passage (76) is a first passage. Wu fails to disclose wherein the second microelectronic device further includes a second passage extending through the second die and the second bond-pad, and wherein the second passage is completely filled with a third conductive material. Kim teaches a first microelectronic device (Fig 16, 46) with a first passage extending through a first bond pad (31) including a first conductive material

(52) and a second conductive material (54) and a second microelectronic device (see Fig 17) further including a second passage extending through the second die and a second bond-pad where the second passage is completely filled with a third conductive material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to include a second passage in the second microelectronic device as taught by Kim in order to provide interconnection for the devices.

Response to Arguments

Applicant's arguments filed 08/13/2009 have been fully considered but they are not persuasive.

Applicant argues (Page 12) that Wu fails to disclose a first conductive material deposited in a first portion of the passage to form a conductive plug and a second conductive material deposited in a second portion of the passage in contact with the conductive plug. The Examiner maintains the position that Wu's solder ball 90 shown in Figure 2F forms the first conductive material in a first portion of the passage to form a conductive plug and the reflowed solder, 92, is considered as the second conductive material deposited in a second portion of the passage in contact with the conductive plug as shown in Figure 2G. Applicant's argument that Wu's metal plug 92 is formed integrally with the solder bump 90 is not persuasive because the claims do not require the first and second materials to be different nor do the claims preclude the first and second conductive materials from being formed integrally. Further, Wu clearly shows

the delineation of two separate conductive portions 90 and 92 in contact with one another in the Figures 2F and 2G.

Applicant's arguments with respect to claims 33 and 39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is (571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. M./
Examiner, Art Unit 2811

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811